IN THE CLAIMS

Please amend the claims as set forth below:

1. (currently amended) A method of operating a content addressable memory (CAM) device, comprising:

receiving an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the input data has a second bit group having a second position in the input data relative to other bit groups;

translating, in response to first translation information, the first bit group from the first position to a different position in a comparand;

translating the second bit group from the second position to a second position of the comparand in response to second translation information;

selecting the first translation information in a first cycle and the second translation information in a second cycle; and

comparing the comparand with data stored in a CAM array.

2. (original) The method of claim 1, further comprising decoding the first translation information.

3. (original) The method of claim 2, further comprising programming the CAM device with the first translation information.

4. (original) The method of claim 2, wherein the translating comprises establishing switch connections between the first position of the input data and the position of the comparand.

5. (canceled)

6. (previously amended) The method of claim 1, further comprising concurrently translating the first and second bit groups into the comparand.

7. (previously amended) The method of claim 1, further comprising sequentially translating the first and second bit groups into the comparand.

8. (canceled)

9. (original) The method of claim 1, further comprising receiving the input data of a first width on an input bus of a second width, the first width being larger than the second width.

10. (original) The method of claim 9, wherein the comparand has a third width being no greater than the second width of the input bus.

11. (original) The method of claim 3, wherein the first translation information determines the position of the comparand register that the first bit group is translated to.

12. (original) The method of claim 3, wherein the first translation information determines which bit group of the plurality of bit groups is to be the first bit group translated to the different position in the comparand.

13. (original) The method of claim 1, wherein receiving comprises receiving the input data from a processor.

14. (previously amended) An apparatus, comprising:

a content addressable memory (CAM) array to receive a comparand; and

a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to a different position in a comparand, the output coupled to the CAM array to transmit the comparand to the CAM array, and wherein the translation circuitry comprises:

a switch circuit;

a storage element to store the translation information; and

a decode circuitry coupled to the storage element to decode the translation information and to establish a connection in the switch circuit between the first position and the position in the comparand.

15. (original) The apparatus of claim 14, further comprising a comparand storage element coupled between the CAM array and the translation circuitry to store the comparand.

16. (canceled)

17. (previously amended) The apparatus of claim 15, wherein the switch circuit comprises at least one multiplexer.

18. (previously amended) The apparatus of claim 14, wherein the switch circuit comprises at least one demultiplexer.

19. (previously amended) The apparatus of claim 14, wherein the switch circuit comprises a cross-bar switch.

20. (canceled)

21. (previously amended) The apparatus of claim 14, further comprising an input bus coupled to the first input of the translation circuit and wherein the switch circuit comprises a plurality of multiplexers each coupled to the input bus.

22. (original) The apparatus of claim 21, wherein the input data has a first width and the input bus has a second width less than the first width of the input data.

23. (original) The apparatus of claim 22, wherein the comparand has a third width being no larger than the second width of the input bus.

24. (original) The apparatus of claim 14, wherein the apparatus further comprises:

a plurality of storage elements, each of the plurality of storage elements to store a portion of the translation information;

selection circuitry coupled to the plurality of storage elements to select from among the plurality of storage elements; and

a decode circuitry coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand.

25. (original) The apparatus of claim 24, wherein each of the plurality of storage elements to store a portion of the translation information for one cycles of a plurality of cycles, and the selection circuitry to select from among the plurality of storage elements based on a particular cycle of the plurality of cycles.

26. (original) The apparatus of claim 25, further comprising a comparand register coupled between the CAM array and the translation circuitry to store the comparand.

27. (original) The apparatus of claim 26, further comprising a processor coupled to the first input of the translation circuitry to transmit the input data.

28. (original) The apparatus of claim 14, further comprising a processor coupled to the first input of the translation circuitry to transmit the input data.

29. (currently amended) An apparatus, comprising:

a content addressable memory (CAM) array having a plurality of CAM blocks each configured to receive a comparand ; and

a plurality of translation circuitry, each of the plurality of translation circuitry coupled to a corresponding one of the plurality of CAM blocks, each translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured

to receive an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to a different position in the comparand received by a respective CAM block, the output coupled to transmit the comparand to the CAM block, wherein each of the plurality of translation circuitry is configured to translate each of the plurality of bit groups ~~over multiple~~in a respective operation cycles.

30. (original) The apparatus of claim 29, wherein each of the plurality of translation circuitry are configured to concurrently transmit the respective comparand to the respective CAM block.

31. (canceled)

32. (original) The apparatus of claim 29, further comprising a plurality of comparand registers, each one of the plurality of comparand registers coupled between a respective one of translation circuitry and a respective one of the CAM blocks to store a respective comparand.

33. (original) The apparatus of claim 29, wherein each of the translation circuitry comprises a switch circuit.

34. (original) The apparatus of claim 33, wherein the switch circuit of at least one of the translation circuitry comprises at least one multiplexer.

35. (original) The apparatus of claim 33, wherein the switch circuit of at least one of the translation circuitry circuits comprises at least one demultiplexer.

36. (original) The apparatus of claim 33, wherein the switch circuit of at least one of the translation circuitry comprises a cross-bar switch.

37. (original) The apparatus of claim 29, wherein each of the translation circuitry further comprises:

a storage element to store the translation information; and

a decode circuitry coupled to the storage element to decode the translation information and to establish a switch circuit connection between the first position and the position in the comparand.

38. (original) The apparatus of claim 36, wherein two or more of the translation circuitry are configured to concurrently establish the switch circuit connection.

39. (currently amended) A content addressable memory (CAM) device, comprising:

a CAM array to receive a comparand;

a switch circuit having an input and an output, the input configured to receive input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, the output coupled to the CAM array to transmit the comparand to the CAM array; ~~and~~

a storage element to store a translation information indicative of a translation of the first bit group from the first position to a different position in the comparand; and

decode circuitry coupled to the storage element to decode the translation information and to establish a switch circuit connection in the switch circuit between the first position and the position in the comparand.

40. (canceled)

41. (original) The CAM device of claim 40, further comprising:

a plurality of additional storage elements, the storage element and each of the plurality of additional storage elements to store a portion of the translation information for one cycle of a plurality of cycles; and

selection circuitry coupled to the storage element and the plurality of additional storage elements to select from among the storage element and the plurality of additional storage

elements based on a particular cycle of the plurality of cycles for transmission to the decode circuitry.

42. (original) The CAM device of claim 41, further comprising a comparand register coupled between the CAM array and the switch to store the comparand.

43. (previously amended) An apparatus comprising:

a content addressable memory (CAM) array; and

means for translating, in response to translation information, a bit group from a position of an input data having a plurality of bit groups to a different position in a comparand, wherein the means for translating comprises:

means for storing the translation information; and

means for decoding the translation information.

44. (canceled)

45. (previously amended) The apparatus of claim 43, wherein the translating comprises means for selecting the translation information from a plurality of translation information.

46. (previously amended) An article comprising a machine readable medium that stores data representing an integrated circuit, comprising:

a content addressable memory (CAM) array to receive a comparand; and

a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to a different position in a comparand, the output coupled to the CAM array to transmit the comparand to the CAM array, wherein the translation circuitry further comprises:

a storage element to store the translation information; and

a decode circuitry coupled to the storage element to decode the translation information and to establish a switch circuit connection between the first position and the position in the comparand.

47. (original) The article of claim 46, wherein the translation circuitry comprises a switch circuit.

48. (canceled)

49. (previously amended) A content addressable memory (CAM) device, comprising:

means for receiving an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the input data has a second bit group having a second position in the input data relative to other bit groups;

means for translating, in response to first translation information, the first bit group from the first position to a different position in a comparand;

means for comparing the comparand with data stored in a CAM array;

means for translating the second bit group from the second position to a second position of the comparand in response to second translation information; and

means for selecting the first translation information in a first cycle and the second translation information in a second cycle.

50. (previously presented) The apparatus of claim 49, further comprising means for decoding the first translation information.

51. (previously presented) The apparatus of claim 50, further comprising means for programming the CAM device with the first translation information.

52. (canceled)

53. (previously amended) The apparatus of claim 49, further comprising means for concurrently translating the first and second bit groups into the comparand.

54. (previously amended) The apparatus of claim 49, further comprising means for sequentially translating the first and second bit groups into the comparand.

55. (canceled)

56. (previously presented) An apparatus, comprising:

a content addressable memory (CAM) array to receive a comparand; and

a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to a different position in a comparand, the output coupled to the CAM array to transmit the comparand to the CAM array, wherein the translation circuitry comprises a switch circuit having at least one demultiplexer.

57. (previously presented) The apparatus of claim 56, wherein the apparatus further comprises:

a plurality of storage elements, each of the plurality of storage elements to store a portion of the translation information;

selection circuitry coupled to the plurality of storage elements to select from among the plurality of storage elements; and

a decode circuitry coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand.

58. (previously presented) The apparatus of claim 57, wherein each of the plurality of storage elements to store a portion of the translation information for one cycles of a plurality of cycles, and the selection circuitry to select from among the plurality of storage elements based on a particular cycle of the plurality of cycles.

59. (previously presented) The apparatus of claim 58, further comprising a comparand register coupled between the CAM array and the translation circuitry to store the comparand.

60. (previously presented) The apparatus of claim 59, further comprising a processor coupled to the first input of the translation circuitry to transmit the input data.